THAT WHICH IS CLAIMED IS:

1. An architecture for distributing supply voltages to a plurality of memory modules supplied through a plurality of charge pump circuits, characterized in that it comprises:

a sorting block bi-directionally connected to said plurality of memory modules from which it receives a plurality of power requests and it is capable of providing a sorting signal of said power requests on the basis of a priority scale in order to drive said plurality of charge pump circuits and distribute supply voltages to said plurality of memory modules.

2. An architecture for distributing supply voltages according to claim 1, characterized in that it further comprises a switching block connected to said plurality of memory modules through a bi-directional bus and to said sorting block to receive at its input said sorting signal.

3. An architecture for distributing supply voltages according to claim 2, characterized in that said sorting block receives, though said bi-directional bus, a power request signal from a memory module of said plurality of modules and a request allocation signal, and it is connected to:

an identification bus of the operation required; and

a priority bus of the request signal.

4. An architecture for distributing supply

voltages according to claim 3, characterized in that said switching block receives at its input said power request signals and it outputs said request allocation signal, and it is connected to said identification bus and priority bus.

5. An architecture for distributing supply voltages according to claim 4, characterized in that said switching block is also bi-directionally connected to a plurality of request decoders to which it provides said power request signal and from which it receives said request allocation signal, said switching block also being connected to said plurality of request decoders through said identification bus.

6. An architecture for distributing supply voltages according to claim 5, characterized in that said request decoders are bi-directionally connected in a multiplexed relationship to a plurality of driving circuits, connected in turn through a further bi-directional bus to said plurality of charge pump circuits.

7. An architecture for distributing supply voltages according to claim 6, characterized in that said plurality of request decoders provides through said further bi-directional bus the following signals:

an activation signal of a corresponding charge pump circuit; and

a stand-by mode signal of a corresponding charge pump circuit.

8. An architecture for distributing supply voltages according to claim 7, characterized in that said plurality of request decoders receives through a further bi-directional bus a validity signal bringing the information that the charge pump has reached the desired value.

9. An architecture for distributing supply voltages according to claim 8, characterized in that said plurality of driving circuits manages the power down and stand-by conditions of said plurality of charge pump circuits by limiting said power requests performed by each charge pump circuit under said highest value allowed.

10. An architecture for distributing supply voltages according to claim 6, characterized in that it is software-configurable.

11. An architecture for distributing supply voltages according to claim 1, characterized in that said sorting block processes said power requests received from said plurality of modules on the basis of the following rules:

request state, the request being already active or a new request;

priority information; and

position of a module which has performed said power request.

12. An architecture for distributing supply voltages according to claim 11, characterized in that

said rules comprise a priority classification of requests received from different modules of said plurality of memory modules.

13. An architecture for distributing supply voltages according to claim 1, characterized in that it processes said power requests received from said plurality of memory modules in a single cycle of a clock signal.